

### **Amendments to the Claims**

This listing of claims will replace all prior versions, and listings of claims in the application:

#### **Listing of Claims:**

Claim 1 (Currently Amended): A stacked semiconductor device consisting of a first semiconductor device having outside electrode terminals on a lower surface thereof, a second semiconductor device electrically connected with said first semiconductor device and secured on said first semiconductor device, said first semiconductor device comprising:

- a first semiconductor substrate;
- first circuit elements at a first main surface of said first semiconductor substrate;
- a first multilayer wiring part on said first circuit elements and configured of a first wiring electrically connected with said first circuit elements and a first insulating material layer, the first wiring and the first insulating material layer being stacked alternately with the first insulating material layer being an uppermost layer;
- a first insulating layer for covering said first insulating material layer of said first multilayer wiring part and provided ~~[[all]]~~ over the first main surface of said first semiconductor substrate, said first insulating layer is a support member of said first semiconductor substrate;

a second insulating layer for covering a second main surface of said first semiconductor substrate that is opposite the first main surface of said first semiconductor substrate;

a plurality of first post electrodes on said first wiring of said first multilayer wiring part and each having a top surface and side surfaces, the top surfaces of said first post electrodes exposed from a surface of said first insulating layer and all the side surfaces of said first post electrodes covered by said first insulating layer;

a plurality of first through-type electrodes penetrating from a specified depth of said first multilayer wiring part to a surface of said second insulating layer through said first semiconductor substrate, said first through-type electrodes insulating from said first semiconductor substrate by a first insulating film and connected with said first wiring of said first multilayer wiring part; and

said outside electrode terminals connected to said first through-type electrodes,  
said second semiconductor device comprising  
a second semiconductor substrate;

second circuit elements formed at a first main surface of said second semiconductor substrate;

a second multilayer wiring part on said second circuit elements and configured of a second wiring electrically connected with said second circuit elements and a second insulating material layer, the second wiring and the second insulating material layer being stacked alternately with the second insulating material layer being an uppermost

layer;

a third insulating layer for covering said second insulating material layer of said second multilayer wiring part and provided ~~[[all]]~~ over the first main surface of said second semiconductor substrate, said third insulating layer is a support member of said second semiconductor substrate;

a fourth insulating layer for covering a second main surface of said second semiconductor substrate that is opposite the first main surface of said second semiconductor substrate; and

at least second post electrodes on said second wiring of said second multilayer wiring part and each having a top surface and side surfaces, the top surfaces of said second post electrodes exposed from a surface of said third insulating layer and all the side surfaces of the second post electrodes covered by said third insulating layer, or a plurality of second through-type electrodes penetrating from a specified depth of said second multilayer wiring part to a surface of said fourth insulating layer through said second semiconductor substrate, said second through-type electrodes insulated from said second semiconductor substrate by a second insulating film and connected with said second wiring of said second multilayer wiring part,

in said first semiconductor device, said first post electrodes or said first through-type electrodes are at the lower surface thereof and are provided with said outside electrode terminals, and

said second through-type electrodes or said second post electrodes at a lower

surface of said second semiconductor device are electrically connected with said first post electrodes or said first through-type electrodes at an upper surface of said first semiconductor device through joints.

Claim 2 (Currently Amended): The stacked semiconductor device according to claim 1, having a third semiconductor device stacked and secured between said first semiconductor device and said second semiconductor device, wherein said third semiconductor device comprises:

- a third semiconductor substrate;

- third circuit elements at a first main surface of said third semiconductor substrate;

- a third multilayer wiring part on said third circuit elements and configured of a third wiring electrically connected with said third circuit elements and a third insulating material layer, the third wiring and the third insulating material layer being stacked alternately with the third insulating material layer being an uppermost layer;

- a fifth insulating layer for covering said third insulating material layer of said third multilayer wiring part and provided ~~[[all]]~~ over the first main surface of said third semiconductor substrate, said fifth insulating layer is a support member of said third semiconductor substrate;

- a sixth insulating layer for covering a second main surface of said third semiconductor substrate that is opposite the first main surface of said third

semiconductor substrate;

a plurality of third post electrodes on said third wiring of said third multilayer wiring part and each having a top surface and side surfaces, the top surfaces of said third post electrodes exposed from a surface of said fifth insulating layer and all the side surfaces of said third post electrodes covered by said fifth insulating layer;

a plurality of third through-type electrodes penetrating from a specified depth of said third multilayer wiring part to a surface of said sixth insulating layer through said third semiconductor substrate, said third through-type electrodes insulated from said third semiconductor substrate by a third insulating film and connected with said third wiring of said third multilayer wiring part, and

the third post electrodes or the third through-type electrodes on upper/lower surfaces of said third semiconductor device are electrically connected with the first post electrodes or the first through-type electrodes of the first semiconductor device at an upper stage side and the second semiconductor device at a lower stage side through joints.

Claim 3 (Previously Presented): The stacked semiconductor device according to claim 1, wherein said first and second semiconductor devices are disposed as a single body, have a same size, and overlap each other.

Claim 4 (Previously Presented): The stacked semiconductor device according to claim 1, comprising a plurality of said second semiconductor devices that are smaller than said first semiconductor device, and are disposed and secured in parallel on said first semiconductor device.

Claim 5 (Previously Presented): The stacked semiconductor device according to claim 1, wherein the first through-type electrodes or the first post electrodes at an upper surface of said first semiconductor device and the second through-type electrodes or the second post electrodes at a lower surface of said second semiconductor device are brought into correspondence and are electrically connected respectively through said joints.

Claim 6 (Previously Presented): The stacked semiconductor device according to claim 1, wherein said joints comprise metal joining.

Claim 7 (Previously Presented): The stacked semiconductor device according to claim 1, wherein said first and second post electrodes comprise a plating film, stud bump electrodes or a CVD film.

Claim 8 (Previously Presented): The stacked semiconductor device according to claim 1, further comprising a metal plate having insulating holes and disposed between said

first semiconductor device and said second semiconductor device,

wherein in a portion of said insulating holes, first ones of said first through-type electrodes or said first post electrodes at an upper surface of said first semiconductor device are electrically connected with first ones of said second through-type electrodes or said second post electrodes at a lower surface of said second semiconductor device through said joints in a state without contacting said metal plate, and second ones of said first through-type electrodes and said first post electrodes of said first semiconductor device and second ones of said second through-type electrodes and said second post electrodes of said second semiconductor device that face said metal plate are electrically connected with said metal plate through said joints.

Claim 9 (Previously Presented): The stacked semiconductor device according to claim 8, wherein the second ones of said first and second through-type electrodes or said first and second post electrodes are provided with a power supply potential or a ground potential through said metal plate.

Claim 10 (Previously Presented): The stacked semiconductor device according to claim 1, wherein one of said first and second semiconductor substrates is a silicon substrate, and another of said first and second semiconductor substrates is a compound semiconductor substrate.

Claim 11 (Previously Presented): The stacked semiconductor device according to claim 1, wherein said first and second through-type electrodes and said first and second post electrodes comprise copper, tungsten, titanium, nickel, aluminum or an alloy thereof.

Claim 12 (Previously Presented): The stacked semiconductor device according to claim 1, wherein a gap between said first semiconductor device and said second semiconductor device is filled with an insulating resin.

Claim 13 (Previously Presented): The stacked semiconductor device according to claim 1, wherein said first and second semiconductor devices respectively have the first and second post electrodes exposed in surfaces of said first and third insulating layers, and said first and second through-type electrodes exposed in surfaces of said second and fourth insulating layers, and said first and second through-type electrodes are formed at exposed ends of specified ones of said first and second post electrodes or said first and second through-type electrodes located in an upper surface.

Claim 14 (Previously Presented): The stacked semiconductor device according to claim 1, wherein said first and second post electrodes have larger diameter than said first and second through-type electrodes.

Claim 15 (Previously Presented): The stacked semiconductor device according to claim 1, wherein said first and second circuit elements are active elements and passive elements.

Claim 16 (Previously Presented): The stacked semiconductor device according to claim 1, wherein said first and second semiconductor substrates have a thickness of around 5 to 50  $\mu\text{m}$ , and said first and third insulating layers have a thickness of around 20 to 100  $\mu\text{m}$ .

Claim 17 (Currently Amended): A semiconductor device comprising:

- a semiconductor substrate;
- circuit elements at a first main surface side of said semiconductor substrate;
- a multilayer wiring part on said circuit elements and configured of a wiring electrically connected with said circuit elements and an insulating layer, the wiring and the insulating layer being stacked alternately with the insulating layer being an uppermost layer;
- a first insulating layer for covering said insulating layer of said multilayer wiring part and provided ~~[[all]]~~ over the first main surface of said semiconductor substrate, said first insulating layer is a support member of said semiconductor substrate;
- a second insulating layer for covering a second main surface of said semiconductor substrate that is opposite the first main surface;

a plurality of post electrodes on said wiring of said multilayer wiring part and each having a top surface and side surfaces, the top surfaces exposed from a surface of said first insulating layer and all the side surfaces covered by said first insulating layer; and

a plurality of through-type electrodes penetrating from a specified depth of said multilayer wiring part to a surface of said second insulating layer through said semiconductor substrate, said through-type electrodes insulated from said semiconductor substrate by an insulating film and connected with said wiring of said multilayer wiring part.

Claim 18 (Previously Presented): The semiconductor device according to claim 17, further comprising protruding electrodes at exposed ends of specified ones of said post electrodes and said through-type electrodes.

Claim 19 (Previously Presented): The semiconductor device according to claim 17, wherein said post electrodes have larger diameter than said through-type electrodes.

Claim 20 (Previously Presented): The semiconductor device according to claim 17, wherein said post electrodes are comprised of a plating film, stud bump electrodes or a CVD film.

Claim 21 (Previously Presented): The semiconductor device according to claim 17, wherein said through-type electrodes and said post electrodes are comprised of copper, tungsten, titanium, nickel, aluminum or an alloy thereof.

Claim 22 (Previously Presented): The semiconductor device according to claim 17, wherein said circuit elements are active elements and passive elements.

Claim 23 (Previously Presented): The semiconductor device according to claim 17, wherein said semiconductor substrate has a thickness of around 5 to 50  $\mu\text{m}$ , and said first insulating layer has thickness of around 20 to 100  $\mu\text{m}$ .

Claims 24 – 46 (Canceled)

Claim 47 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate having first and second main surfaces, and a circuit on the first main surface;

a multilayer wiring part including an insulating layer and a wiring pattern electrically connected with the circuit, the insulating layer and the wiring pattern disposed over the first main surface alternately with respect to each other;

a first insulating layer on an uppermost layer of said multilayer wiring part over the first main surface of said semiconductor substrate, said first insulating layer is a

support member of said semiconductor substrate;

a second insulating layer over the second main surface;

a first electrode over the first main surface, the first electrode having top and side surfaces and electrically connected with a part of the wiring pattern, the top surface being exposed from a surface of said first insulating layer and all the side surfaces being covered with said first insulating layer; and

a second electrode formed on an inner wall of a through-via which penetrates from the first main surface to the second main surface.

Claim 48 (Previously Presented): The semiconductor device according to claim 47, wherein said first insulating layer is thicker than the insulating layer of said multilayer wiring part.

Claim 49 (Previously Presented): The semiconductor device according to claim 47, wherein said first insulating layer is thicker than said semiconductor substrate.

Claim 50 (Previously Presented): The semiconductor device according to claim 47, wherein said first insulating layer comprises encapsulation resin.

Claim 51 (Previously Presented): The semiconductor device according to claim 47, wherein said second electrode is a through-type electrode.